REMARKS

Claims 1-25 are pending in the application. Claims 1, 2 and 4-25 are allowed.

An Information Disclosure Statement and 1449 form was filed concurrently with the present application. A copy of the 1449 form, initialed showing consideration of the references, was not returned in the previous Office Action. A courtesy copy of the 1449 form is again submitted herewith. It is respectfully requested an initialed copy be returned to applicant.

Claim 3 is amended herein to clarify the present invention.

Claim 3 is rejected under 35 U.S.C. § 102(b) as being anticipated by Iwasa et al. (U.S. 5,522,058) (Iwasa).

In the Office Action it is asserted that a sharing indication line 18 of Iwasa corresponds to a signal line of applicant's claim 3 and a cache memory control section of claim 3 is taught by the Iwasa disclosure at column 36, lines 10-30. Applicant respectfully disagrees for at least the following reasons:

The sharing indication line 18 of Iwasa is provided for transmitting a signal indicative of whether or not the address to be accessed is shared by the cache memory on the processor board.

The signal line of applicant's claim 3 is provided for transmitting data and address to the main memory. Therefore, the signal line of claim 3 is different from the sharing indication line 18 of Iwasa with regard to the purpose of the signal transmitted therethrough.

With regard to the cache memory control section of applicant's claim 3, Iwasa disclose two lines connected with a main memory 3 and a cache 2 in Fig. 2. One of the lines is an internal bus 5 connected with the main memory 3, the sharing management unit 4, and the cache 2, the other is a bus line connected only with the cache 2 and the main memory 3.

However Iwasa does not disclose a connection of the internal bus 5 with the main memory 3 in Fig. 4, and does not disclose an operation of the internal bus 5 to the main memory 3 when a write back command is issued in column 36, lines 10-30 of Iwasa.

Therefore, the internal bus 5 is not provided for writing back data into the main memory 3 when the write back command is issued, and data can not be written back into the main memory 3 and the cache 2 in Fig. 3 is kept locked.

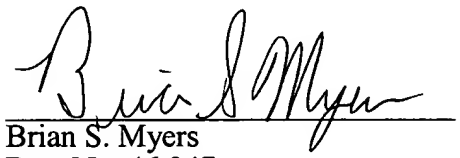
In contrast to the disclosure in Iwasa, applicant's claim 3 provides that the first bus and the signal line are connected with the main memory and the cache control unit. The first bus is provided for reading data from the main memory and writing data into the main memory by the cache control unit of claim 3 when the write back command is not outputted to a second bus. The signal line is provided for writing back data into the main memory by the cache control unit when the write back command is outputted to the second bus, and data can be written into the main memory even if the first bus is kept locked.

For at least the foregoing reasons it is respectfully requested the rejection of applicant's claim 3 be withdrawn and the claim be placed in condition for allowance.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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